CURRICULUM VITAE

PERSONAL DETAILS

Name	NGUYEN VAN TANG
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Date of birth	April 02, 1980
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WORKING INTERESTS

Formal methods, Software Development, and Teaching, IT Manager: Software requirement analysis and design, software verification and validation, system modeling and model checking, computer algorithms, safety-critical systems verification, model checking for security, application of mathematics and formal methods to software development.

LANGUAGE SKILL

1. **Vietnamese:** Mother Tongue
2. **English:** Fluently
3. **Japanese:** Communication N3

EDUCATION

Japan Advanced Institute of Science and Technology (Ph.D. in Computer Science)	From 04/2006 To 03/2009
Vietnam National University, Hanoi (M.Sc. in Computer Science)	From 09/2003 To 12/2005
Vietnam National University of Education (Bachelor in Maths and Informatics)	From 09/1998 To 08/2002
Vinh University Pupil for Special class of Mathematics	From 09/1995 To 06/1998

EMPLOYMENT HISTORY

Duration	Title/Name of Institution
11/2015 – date	- Researcher at Institute of Technology, Lecturer at Faculty of Information Technology, Hanoi University of Industry.
9-10/2015	Manager/Senior Engineer, Samsung Electronics Vietnam.
2/2014 – 8/2015	- Researcher & Manager at The Office of National Programs on Science and Technology, Ministry of Science and Technology, Vietnam. Invited lecturer at University of Science and Technology Hanoi (USTH), and FPT University.
3/2013 – 2/2014	Lecturer at Hanoi University ò Industry
4/2009 – 3/2013	Postdoctoral Researcher at Research Institute for Secure Systems, National Institute of Advanced Industrial Science and Technology – Japan. http://www.aist.go.jp/
8-9/2012	Invited Researcher/Lecturer at Department of Computer Science, Maryland University, USA.
2-3/2010	Invited Researcher at Department of Computer Science, Bath University, UK.
4/2006 – 3/2009	Research assistant at Trust e-Society Research Center, Japan Advanced Institute of Science and Technology – Japan. http://www.jaist.ac.jp/
6/2003 – 3/2006	Researcher at Hanoi Institute of Information Technology
9/2002 –	Teaching Assistant Hanoi University of Education

HONORS AND AWARDS

- Awarded excellent result for PhD. program. Japan Advanced Institute of Science and Technology, March 2009.
- Research Foundation for the Electrotechnology of Chubu Grant, 2008
- Japanese Government Scholarship, COE program, 2006-2009
- National Research Foundation for Master Students, Hanoi University of Science, 2003-2005
- Top 5/150 of bachelor's degree
- Vietnamese Government Scholarship, 1998-2002 for undergraduate students, 1995-1998 for high school pupil

COMPUTER SKILLS

No	Skills	Description
1	**Programming Languages**	Java/J2EE (7+year), C/C++ (2+ year), Haskell, Pascal.
2	**Software development methodology**	UML, Object-oriented software development, Pattern design, Agile method, SEMAT.
2	**Database**	SQL, MySQL, NoSQL
3	**Modeling Tools**	UML/Rational Rose, RAISE specification languages, Object-oriented VDM modeling and specification languages,
4	**Software Verification/Testing**	• **VDM:** Applied VDM Tool to model and test a Train Fare Calculation System using VDM++ specification languages. • **Automated testing:** JUnit, Selenium 2.0. • **SPIN model checker:** Applied SPIN to model, simulate and verify safety properties for a core algorithm of the real-time operating system. • **CPROVER:** A tool for automated checking C/C++ source code. • **Agda:** Applied Agda to model and prove reliability properties of a Train Fare Calculation System. • **SMV/NuSMV model checker, SAT/SMT Solvers: YICES**. • **Proablilistic Interpreter System Modeling (PRISM)**: Studied PRISM on the webpage www.prismmodelchechker.org • **UPPAAL**: Applied UPPAAL to model and verify a case study of real-time gas-control systems.
5	**Operating Systems**	Microsoft Windows XP/2000, Linux/Cygwin
6	**Management Tools**	MS Project 2010

INDUSTRIAL R&D EXPERIENCE

I had participated in some R&D projects with Japanese IT companies as below:

No	Project Name	Fund & Time	Contributions
1	Modeling and Validating A Train Fare Calculation and Adjustment System	A collaborative research project between AIST and OMRON. April, 2009 - December, 2010.	- **My role:** Modeling and testing the train fare calculation and adjustment system using VDM++. Write the connection module between VDM++ and C/C++. Transform test data in XML format to VDM format. Modeling and specifying the system in Agda Proof Assistant. Prove reliability properties for the system in Agda. Develop the testing system in Java/C++ and VDM++. - **Project achievement:** In this project, we have successfully modeled and tested for the whole fare calculation and adjustment system against over 10 million testcase. We detected many inconsistencies and omission in the specification document in the modeling phase. For the test phase, we performed testing and detected a subtle error in design of the system. Our project has been evaluated successfully by Japanese railways companies. And now, the project becomes a noticeable example of applying formal methods to Industry in Japan.
2	Automated Testcase generation for automotive operating systems	A joint project with Toshiba. Duration: March, 2011 – September, 2012.	- **My role:** Join to develop an algorithm to generate test cases from functional specification of system described as feature trees using SAT/SMT solver and Pair-wise testing techniques. - **Project achievement:** We have developed a method and tool for automated test case generation

			so-called FOT tool. The method and tool were registered as a patent in Japan. The tool was used by Toshiba and several IT companies on the field of embedded systems.
3	Study specification language and automatic test-cases generation for embedded networked systems	A joint research project between AIST and Daikin Industries. Duration: April, 2012 – March, 2013.	- **My role:** Analyze and study how to use model checking to generate test sequences for Network Airconditioning Systems. - **Project achievement:** The project resulted in a tool for test case/sequence generation so-called SENS. The tool was used by Daikin Industries for their QA purposes.
4	Formal verification and testing of real-time embedded operating systems	A joint project between AIST and LETech company. Duration: November, 2011 - March, 2013.	- **My role:** Modeling the algorithm using SPIN and NuSMV model checkers. Reading and checking requirements of the systems. - **Project achievement:** In this project, we have modeled and verified deadlock-free and liveness for kernel (including NMI's management) of the operating systems.
5	Model Checking Embedded System Designs in State Transitions Matrix	A joint project with Fukuoka/IST. January, 2011 - March, 2012. This research is conducted as a program for the "Regional Innovation Cluster (Global Type, the 2nd Stage)" by Ministry of Education, Culture, Sports, Science and Technology (MEXT), Japan.	- **My role:** Study state transition matrix, study specification patterns, write a tool called SpecSelector in Java that allows users to select specification patterns and build required properties conveniently. - **Project achievement:** In this project, we have created two products: (1) A model checker so-called Garakabu2 for state-transition matrix using SAT solver as back-end engine; (2) A SpecEditor- a tool for editing pattern specifications that helps engineers to specify/edit LTL requirements.
6	JSPS Bilateral Joint Research Projects	Funded by the Japan Society for the	- **My role:** A principal researcher as well as a connector to establish research exchange and relationship

	between AIST/CVS-Japan and VAST/IoIT-Vietnam: Training Software Quality Assurance for Embedded systems.	Promotion of Science (JSPS) and VAST/Vietnam. Duration: 8/2011– 8/2014.	between AIST/Japan and Vietnamese institutions and companies. - **Project achievement:** We have successfully organize seminars/exchange trip between two countries (Japan and Vietnam). By doing so, we do joint research and create a network/relationship of research institutions and IT companies.
7	National Industrialized High-Technology Project: Optimization and Big data for Logistics and Transportation Problems.	Funded by Vietnamese Government: Ministry of Industry and Trade, Ministry of Science and Technology. Duration: 7/2015-6/2017.	- **My role:** A principal researcher, project leader and manager.

ACADEMIC R&D AND PUBLICATIONS

Selected Publications

1. Nguyen Van Tang, Daisuke Souma, Goro Hatayama, Hitoshi Ohsaki. **A Method for the Development of Train Fare Calculation and Adjustment Systems Using VDM++**. A chapter to appear in the book: “Railways: Types, Design, and Safety Issues”. Editors: Cacilie Reinhardt and Klaus Shroeder, ISBN: 978-1-62417-139-0. Nova Science Publishers, New York, America, 2013.

   Abstract: The Train Fare Calculation and Adjustment System (TFCAS), developed by the OMRON Corporation, is a large-scale and complex system that helps passengers buy tickets and adjust their train fare on the railways across Japan. In this work, we present the results and experiences gained in a collaborative research project between AIST and OMRON, in which VDM++ has been applied to formalize TFCAS's specifications and validate its consistency as well as reliability properties. An executable VDM++ model can be used to raise the level of the quality of the informal system specification, the efficiency of existing system test-suites, and the quality of real implementation. The application of VDM++ enables us to detect 32 erroneous issues in the original informal specification document. Moreover, we also show how the development process can be improved in a front-loading manner using the formal method VDM++.

2. Nguyen Van Tang and Hitoshi Ohsaki. **On Model Checking for Visibly**

Pushdown Automata. In the Proc. of *the 6th International Conference on Language and Automata Theory and Applications (LATA 2012)*, A Coruna, Spain, March 2012. Volume 7183, pp. 428-440. Lecture Notes in Computer Science, Springer-Verlag.

Abstract: Visibly pushdown automata [Alur and Madhusudan, 2004] are pushdown automata whose stack behavior (i.e., whether to execute push, pop, or no stack operation) is completely determined by the input symbol according to a fixed partition of the input alphabet. The class of visibly pushdown automata enjoys many good properties similar to those of the class of finite automata. The main reason for this being is that, each nondeterministic VPA can be transformed into an equivalent deterministic one. Therefore, checking context-free properties of pushdown models is decidable as long as the calls and returns are made visible. As a result, visibly pushdown automata have turned out to be useful in some context, e.g., as automaton model for processing XML streams, and as AOP protocols for component-based systems. To check universality for a nondeterministic VPA M over its alphabet $\sum$ (that is, to check if L(M)=$\sum^*$, the standard method is first to make it complete, determinize it, complement it, and then check it for emptiness. To check the inclusion problem L(M) $\subseteq$ L(N), the standard method computes the complement of N, takes its intersection with M and then, checks for emptiness. This is costly as computing the complement necessitates a full determinization. This explosion is in some senses inevitable, because determinization for VPA requires exponential time blowup. This raises a natural question: Are there methods to efficiently implement decision procedures like universality (or inclusion) checking for VPA.

In this paper, we introduced on-the-fly algorithms to test universality and inclusion problems of visibly pushdown automata. We implemented the proposed algorithms in a prototype tool. We conducted experiments on randomly generated VPA. The experimental results show that the proposed method outperforms the standard one by several orders of magnitude.

3. Nguyen Van Tang and Mizuhito Ogawa. **Event-Clock Visibly Pushdown Automata**. In the *Proceedings of the 35th International Conference on Current Trends in Theory and Practice of Computer Science (SOFSEM'09)*, LNCS 5404, pp. 558-569, Spindler¨uv Ml´yn, Czech Republic, January 2009.

Abstract: In this paper, we introduced the class of event-clock visibly pushdown automata (ECVPAs) as an extension of event-clock automata. The class of ECVPAs, on one hand, can model simple real-time pushdown systems and, on the other hand, is determinizable and closed under Boolean operations. We also show that for a timed visibly pushdown automaton A and an ECVPA B, the inclusion problem L(A) $\subseteq$ L(B) is decidable.

Book chapters and Journals

1. Yoriyuki Yamagata, Weiqiang Kong, Akira Fukuda, Nguyen Van Tang, Hitoshi Ohsaki, and Kenji Taguchi. **Formal Semantics of Extended Hierarchical State Transition Matrix by CSP: Extended version.** In Formal Aspects of Computing (SCI), 26(5), 943-962, Springer-Verlag Publishers, 2014.
2. Eun-hye Choi, Takahiro Ando, Hideaki Nishihara, Nguyen Van Tang, Cyrille

Artho, Hitoshi Ohsaki. **TestTraces: Formal Specification based Automatic Test Generation for Embedded Network Systems.** In a special issue of "Software Engineering and Statistical Software Quality Assurance", Journal of Applied Mathematics (SCI), 909761:1-21, Hindawi Publisher 2014.

3. Nguyen Van Tang, Daisuke Souma, Goro Hatayama, Hitoshi Ohsaki. **A Method for the Development of Train Fare Calculation and Adjustment Systems Using VDM++**. A chapter to appear in the book: “Railways: Types, Design, and Safety Issues”. Editors: Cacilie Reinhardt and Klaus Shroeder, ISBN: 978-1-62417-139-0. Nova Science Publishers, New York, America, 2013.

4. Nguyen Van Tang and Hitoshi Ohsaki. **On-the-fly Checking Universality and Inclusion Problems of Visibly Pushdown Automata**. Special Section on Mathematical Systems Science and its Applications. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences (ISI),Vol.E94-A,No.12,pp. 2794-2801,December 2011.

5. Koichi Kobayashi, Kunihiko Hiraishi, and Nguyen Van Tang. **Approximate Algorithm for Hybrid Model Predictive Control with Time-Varying Reference**. IEICE Transactions on Fundamentals of Electronics, Communications, and Computer Sciences (ISI). Volume E92-A, No. 8, pp. 2046-2052, 2009.

6. Nguyen Van Tang and Mizuhito Ogawa. **An Improvement on Decision Procedure for Inclusion Problem of Superdeterministic Pushdown Automata**. *IPSJ Transactions on Programming*, Vol. 1(1), pp. 36-46, June 2008.

Refereed Conference Proceedings

7. Do Ngoc Thi Bich, Takashi Kitamura, Nguyen Van Tang, Hitoshi Ohsaki. **Automated Test Case Generation Using Feature-Oriented and n-Wise Testing**. In the proceedings of the fourth international symposium on information and communication technology (SoICT 2013), pp: 275-284.

8. Yoriyuki Yamagata, Weiqiang Kong, Akira Fukuda, Nguyen Van Tang, Hitoshi Ohsaki, and Kenji Taguchi. **Formal Semantics of Extended Hierarchical State Transition Matrix by CSP**. In the Proc. of *the 5th International Workshop on UML& Formal Methods 2012*, August 2012, Paris. In ACM Software Engineering Notes, 37(4), 1-8, 2012.

9. Nguyen Van Tang and Hitoshi Ohsaki. **On Model Checking for Visibly Pushdown Automata**. In the Proc. of *the 6th International Conference on Language and Automata Theory and Applications (LATA 2012)*, A Coruna, Spain, March 2012. Volume 7183, pp. 428-440. Lecture Notes in Computer Science, Springer-Verlag.
10. N. V. Tang, D.Souma, G. Hatayama, H. Ohsaki. **Modeling and Validating Train Fare Calculation and Adjustment System Using VDM++**. In the Proc. of *the fourth international conference on Verified Software: Theories, Tools, and Experiments (VSTTE 2012)*. A co-located event of *the 39th ACM*

SIGPLAN-SIGACT Symposium on Principles of Programming Languages (POPL 2012), January 22-29, Philadelphia, USA. Lecture Notes in Computer Science: R. Joshi, P. Muller and A. Podelski (Eds.), Volume 7152, pp. 163 - 178, Springer-Verlag.

11. Nguyen Van Tang. **A Tighter Bound for Determinization of Visibly Pushdown Automata**. In the *Proceedings of the 11th International Workshop on Verification of Infinite-State Systems (INFINITY'09). A Satellite Event of the 20th International Conference on Concurrency Theory (CONCUR'09)*, Bologna, Italy, September 2009. Electronic Proceedings of Theoretical Computer Science, Volume. 10, pp. 62-76, 2009.

12. Nguyen Van Tang and Mizuhito Ogawa. **Event-Clock Visibly Pushdown Automata**. In the *Proceedings of the 35th International Conference on Current Trends in Theory and Practice of Computer Science (SOFSEM'09)*, LNCS 5404, pp. 558-569, Spindler¨uv Ml´yn, Czech Republic, January 2009.

13. Koichi Kobayashi, Nguyen Van Tang, and Kunihiko Hiraishi. **Precomputation Based Approximate Algorithm for Model Predictive Control of Hybrid Systems**. In the *Proceedings of the 23rd International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC'08)*, pp. 913-916, July 2008.
14. Nguyen Van Tang, Dang Van Hung, and Mizuhito Ogawa. **Modeling Urgency in Component-Based Real-time Systems**. In the *Proceedings of the 11th Annual Asian Computing Science Conference (ASIAN'06)*, LNCS 4435, pp. 249-256, Tokyo, Japan, 2006.
15. Nguyen Van Tang, Hitoshi Ohsaki, and et al. **Formal Verification of A Train Fare Calculation System by The Agda Proof Assistant.** In the Proceedings of the first International Workshop on Simulation Based Development of Certified Embedded Systems (SBDCES'09)}, Awaji, Japan, October 2009.

TEACHING EXPERIENCES

No.	Course Name	University	Course's Language	Level	Time
1	Software Engineering for Interactive Media	**Invited lecturer at** University of Science and Technology, Hanoi (An Collaborated University between France and Vietnam) http://www.usth.edu.vn/	English	Graduate	Summer 2013, Autumn 2014
2	Software Quality	**Invited lecturer at**	English	Graduate	Autumn

	Assurance and Testing	FPT University http://www.fpt.edu.vn/			2014
3	Agile Software Development Methods	**Invited lecturer at** FPT University	English	Graduate	Spring 2015
4	Software Verification and Validation: Academy-Industry-Government Collaboration Experience in AIST/Japan	**Guest lecturer at** Department of Computer Science, University of Maryland, USA	English	Graduate	September 22nd -28th , 2012
5	Software Project Management, Software Engineering, Java Programming language	Hanoi University of Industry	Vietnamese	Undergraduate	2013

SOFTWARE TOOLS

- **SpecEditor:** Nguyen Van Tang. A Graphical System for Specifying LTL Requirements of Software Systems. Written in Java.
- **FOT:** A tool for automated test-input generation based on feature tree. Written in Java/C/Haskell.
- **TFC-Tester:** G. Hatayama, D. Souma, N. V. Tang, and H. Ohsaki. A System for Specification and Verification of Japanese Train Fare Calculation Software. Written in VDM++, Java, and C/C++.
- **VPAchecker:** A Prototype Tool for Checking Universality and Inclusion of Visibly Pushdown Automata. The package was written in Java 1.5.0/NetBeans 6.0.
- **iLogis:** A software system for logistics and data analysis of of moving vehicle and transportation.

TALKS AND PROFESSIONAL SERVICES

- Software Verification and Validation: Academy-Industry-Government Collaboration in AIST. Department of Computer Science, University of Maryland, USA, September 6th, 2012.
- Checking Universality and Inclusion for Visibly Pushdown Automata. Seminar at LIAFA Group, University of Paris 7, Paris, France, March 8th, 2012.
- On Model Checking for Visibly Pushdown Automata. LATA 2012, La Coruna, Spain, March 6th, 2012.
- Modeling and Validating the Train Fare Calculation System Using VDM++. VSTTE 2012, Philadelphia, America, January 29th, 2012.
- Industrial Experience of Using Formal Methods for Software Verification in AIST. Seminar at PRECISE Center, Pennsylvania University, Philadelphia January 25th, 2012.
- A Hybrid Approach to Formal Verification of Train Fare Calculation System using Testing and Theorem proving. Video-Conference Seminar. Bath-Swanse University, Bath, UK, March 18th, 2010.
- Precomputation Based Approximate Algorithm for Model Predictive Control of Hybrid Systems. ICT-CSCC'08, Shimonoseki, Yamaguchi, Japan, August 2008.
- Visibly Stack Automata. Tohoku University, Sendai, Japan, November 2007.
- Modeling Urgency in Component-based Real-time Systems. ASIAN'06, NII, Tokyo, December 2006.
- Program Committee for the First International Workshop on Formal Techniques for Safety-Critical Systems (FTSCS 2012), November 12, Kyoto, Japan.
- Program Committee for the Second International Workshop on Formal Techniques for Safety-Critical Systems (FTSCS 2013), October 29, Queenstown, New Zealand 2013.

REFERENCES

1. **Senior Researcher. Dr. Hitoshi Ohsaki**

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   Research Institute for Secure Systems
   National Institute of Advanced Industrial Science and Technology
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